Low voltage DC-to-DC Converter with Wide Input to Output Voltage Ratio

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ABSTRACT - DC-to-DC converters with very low input respectively output voltage ratings have, due to the high current ratings, a relatively low efficiency. Therefore, it is necessary to operate several converter stages in parallel to achieve an acceptable total efficiency. Here, a possible solution for such a converter is presented. The input voltage of a (e.g. a solar buffered) battery (12V or 24V) has to be converted into a DC-voltage of 350V, e.g. for a power transmitter. The total power to be managed is 1kW. In case of a single stage inverter, this leads to about 100A input current (causing peak values in the power switches of up to 200A!). The resulting component stress is very hard and the design is also difficult to handle. To overcome this problem a topology was chosen, which uses several converter stages operating in parallel. All these stages operate at the same transformer leading to an optimal flux exploitation of the core. Figure 1 depicts the realization principle for a two-converter solution. In the case of the 1kW converter described here, four stages are used.

INTRODUCTION

The main disadvantage of the DC-link supply of solar power inverters operating at low DC-input voltages is the extremely high input current. To overcome this, usually several stages must be operated in parallel. Contrary to this, a transformer based current sharing architecture is used in this paper (c.f. Fig. 1).

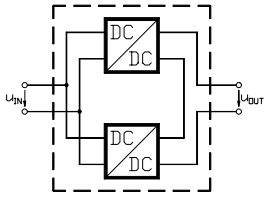

Fig. 1.a. Hard paralleling

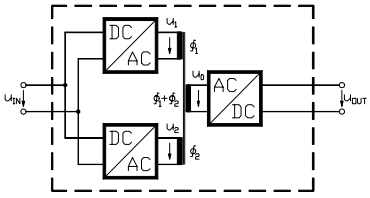

Fig. 1.b. Isolated topology

THE BASIC CONVERTER TOPOLOGY

The primary (low voltage) side of the proposed converter (c.f. Fig. 1b., DC-to-AC section) was realized by the well-known push-pull structure (c.f. Fig. 2) [5].

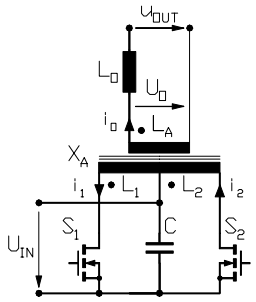

Fig. 2a. Basic converter topology

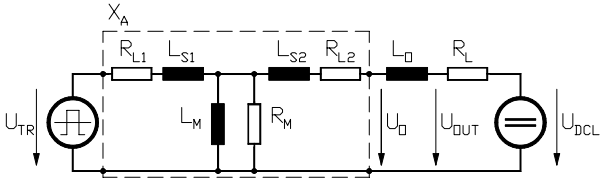

Fig. 2b. The corresponding equivalent circuit (right)

To clarify the operation principle, four different system states can be given (c.f. Fig. 3):

a.) S1 conduction (positive i_1): the input current rises
b.) S1 opened (positive i_2) free-wheeling path over D_2: input current decreasing
c.) S2 conduction (negative i_2): the input current rises
d.) S2 opened (negative i_1) free-wheeling path over D_1: input current decreasing.

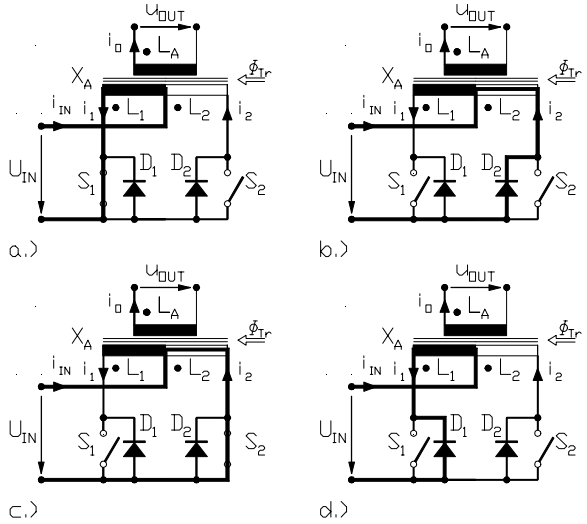

Fig. 3. Operational principle of the basic topology

An idealized transformer is assumed to explain the basic principle. Therefore, the main-inductor L_M and the magnetizing losses (represented by R_M) are neglected. For each operation state the system equations can be given:

$$U_{TR}(=U[L_1]) = +U_{IN} \tag{1}$$

$$U_{IN} - U_{DC} = i_1 \cdot (R_{L1} + R_{L1} + R_O) + \frac{di_1}{dt}(L_{S1} + L_{S1} + L_O) \tag{2}$$

$$i_1 = \frac{U_{IN} - U_{DC}}{R_{L1} + R_{L2} + R_O} \cdot \left(1 - e^{-\frac{R_{L1}+R_{L2}+R_L}{L_{S1}+L_{S2}+L_O}t}\right) + i_{AB} \cdot e^{-\frac{R_{L1}+R_{L2}+R_L}{L_{S1}+L_{S2}+L_O}t} \tag{3}$$

$$U_{TR}(=U[L_1]) = -U_{IN} \tag{4}$$

$$-U_{IN} - U_{DC} = i_1 \cdot (R_{L1} + R_{L1} + R_O) + \frac{di_1}{dt}(L_{S1} + L_{S1} + L_O) \tag{5}$$

$$i_1 = -\frac{U_{IN} + U_{DC}}{R_{L1} + R_{L2} + R_O} \cdot \left(1 - e^{-\frac{R_{L1}+R_{L2}+R_L}{L_{S1}+L_{S2}+L_O}t}\right) + i_{AB} \cdot e^{-\frac{R_{L1}+R_{L2}+R_L}{L_{S1}+L_{S2}+L_O}t} \tag{6}$$

When the current reaches zero (depending on the duty cycle), the diode turns off. The voltage across the primary inductance of the transformer is now zero, until the opposite switch is turned on.
As can be seen from the equivalent circuit Fig. 2, the structure is very similar to the standard buck-converter. A detailed circuit level base simulation was chosen to analyze the component stress.

SIMULATION RESULTS OF THE STANDARD STRUCTURE

The structure given in Fig. 2 was modeled in PSPICE and simulated. For this model a 1:31.6-transformer was used. The simulation results of the topology (input voltage: 12V, load resistance: 1kΩ, duty cycle: 50%) are shown in Fig. 4.

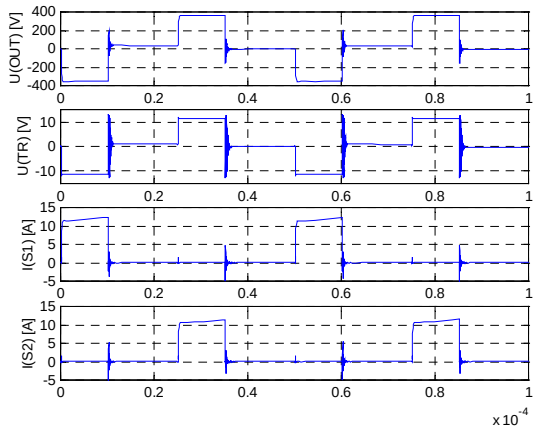

Fig. 4. Simulation: from top to bottom: output voltage, voltage across one primary, current through switch 1 & 2

For the sake of clarity and to show the influence of the magnetizing current, a transformer ratio of 1:1 is chosen in Figs. 5, 6 & 7. Figure 5 shows the simulation results at no load condition of the converter, while Fig. 6 depicts a 12A load condition (1Ω load). The magnetizing current can be seen clearly in both cases.

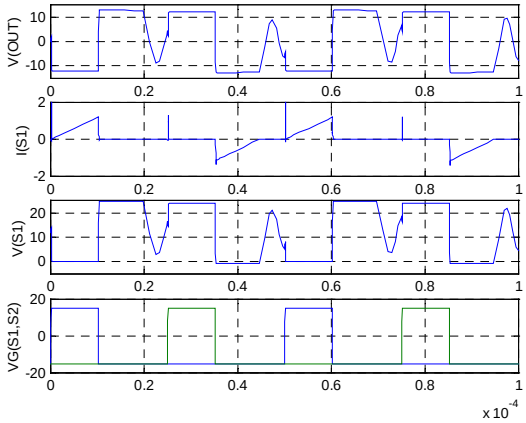

Fig. 5. Simulation from top to bottom: output voltage, transformer current (here magnetizing current), voltage across one switch, control signal of the switches

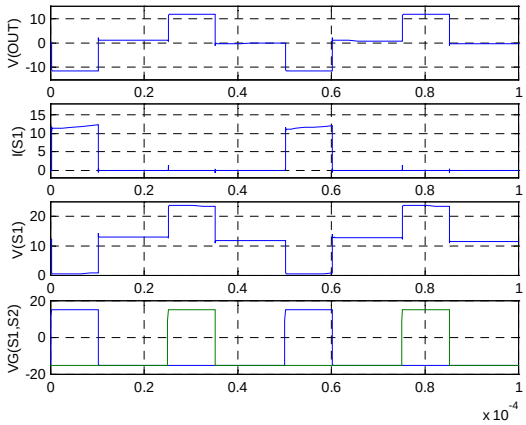

Fig. 6. Simulation from top to bottom: output voltage, transformer current (magnetizing plus transformed load current), voltage across one switch, control signal of the switches. (discontinuous mode).

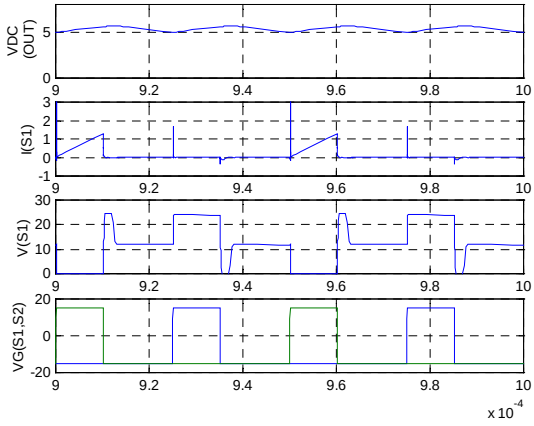

Fig. 7. Simulation from top to bottom: output voltage, switch current (magnetizing plus transformed load current), voltage across one switch, control signal of the switches. (inductive load).

THE CURRENT SHARING CONVERTER TOPOLOGY

The basic topology was used to build the converter system given in Fig. 8. Here two stages are operating in parallel. The model uses three transformers to clarify the operation. The stages A and B are operated with the same clock and the same phase. Depending on the duty cycle for each converter stage, a load sharing can be realized. The simplest way is to use the same control signals for all stages.

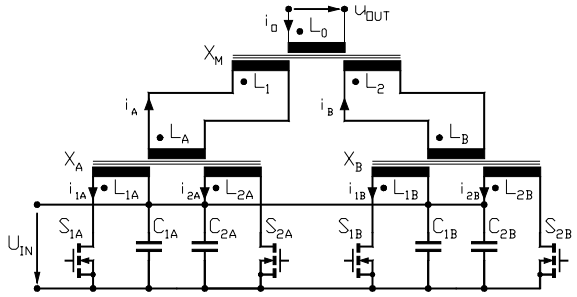

Fig. 8 Current amplifier topology, derived converter model

SIMULATION RESULTS OF THE CURRENT SHARING CONVERTER TOPOLOGY

As one can see from the simulation results (Figs. 9 & 10), the new topology leads to a current sharing between the stages. The resulting current stress in the power semiconductors is divided by the number of operating stages working in parallel. Here also a winding ratio of 1:1 is used for explanation. In Fig. 9 the no load condition and in Fig. 10 an approximately 12A load case (R_L=1Ω) are shown.

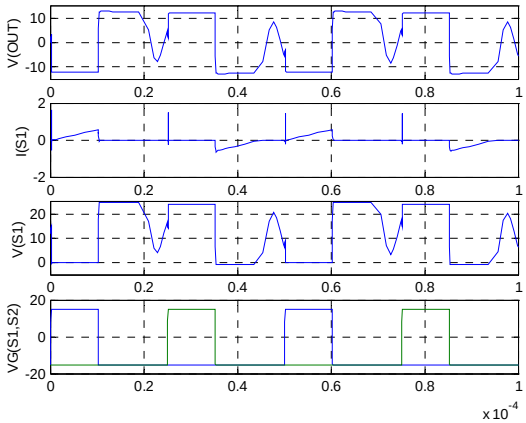

Fig. 9. Simulation from top to bottom: output voltage, transformer current (here magnetizing current), voltage across one switch, control signal of the switches

A major advantage is the insensitivity of the structure in case of down powered stages or stages operating only at a partial load point. This is very useful when applied at solar power inverters, where several solar arrays can easily be connected in parallel operating each array at its special MPP (maximum power point).

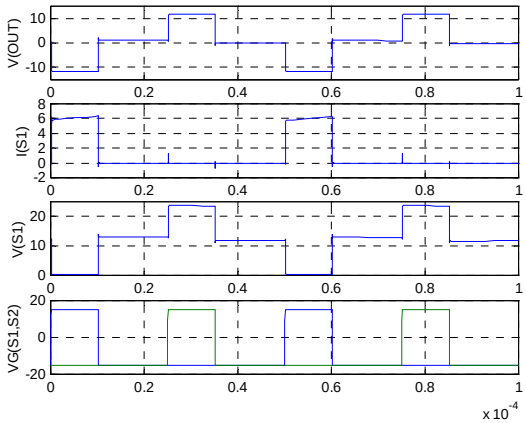

Fig. 10. Simulation from top to bottom: output voltage, transformer current (magnetizing plus transformed load current), voltage across one switch, control signal of the switches

The resulting efficiency of the solution is therefore much better than a global serial or parallel connection of the arrays.

REALIZATION OF THE CONVERTER

The principal topology given in Fig. 6 uses a multiple transformer arrangement. To simplify the topology, an E-core realization is presented here.

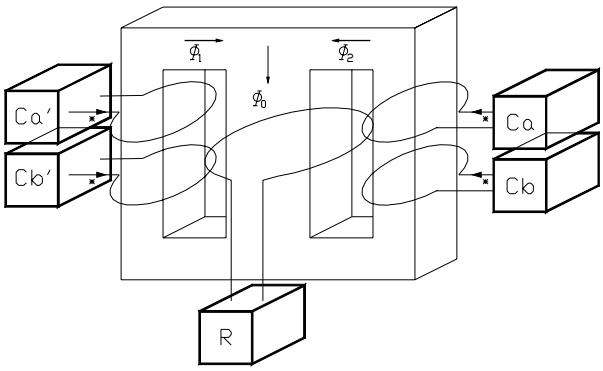

Fig. 11. Inverter topology

As shown in Fig. 11 the arrangement uses converters operating on the left side of a standard E-core and also converters on the right side. The accumulated flux of the transformer is fed through the center leg, where the secondary windings are located, and results in an approximately doubled voltage transfer ratio of this structure in case of symmetry.
When the converters are operated with the same control signals, the flux in the center leg is $\Phi_0 = \Phi_1 + \Phi_2$. This is the normal operation mode. In case of multiple solar arrays, only small differences

in the control signal will occur to keep each array-field at MPP.

In case of asymmetric operation, a different state has to be taken into consideration.
Here only one side of the converter is operating. The resulting flux in the center leg is smaller than the flux generated by the source (e.g. left side: $\Phi_0 \leq \Phi_1$) depending on the relationship of the magnetic resistances due to the different geometric of the center and the outside legs. Only a part of the generated magnetic flux contributes to the output voltage. In this case the voltage transfer ratio of the converter is reduced.
The current sharing can be managed by operating several converters in parallel on the same leg of the core (e.g. *a* and *b* in Fig. 9). In this case the converter current is shared between the single stages. This helps to minimize the current stress in the power semiconductors.

REALIZATION OF THE TRANSFORMER

The practical realization of a converter based on two stages as given in Fig. 6 using an E-core transformer is shown in Fig. 12. The primary windings (a,a', b,b') are realized by a copper tape on the peripheral leg of the core. The secondary side was realized as a conventional multiturn HF-liz coil on the center leg of the core.

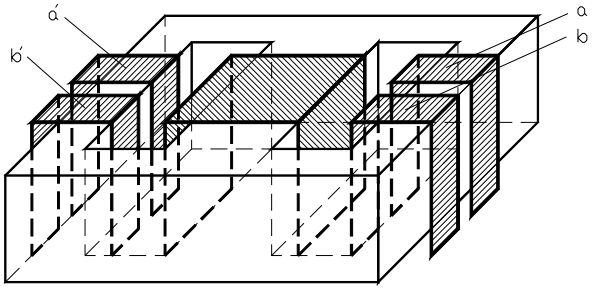

Fig. 12 Transformer schematic

Due to the summation of the magnetic fluxes (Φ_1, Φ_2), the winding voltage on the secondary side is doubled leading to a more effective and compact design.
Another important task is the selection of the rectifier stage. If a center-tapped transformer is used, the voltage ratings of the diodes are more than twice of the nominal output voltage of the converter. This disadvantage can be overcome by two identical secondary sections connected in series. The disadvantage of increased losses, due to the forward voltage of two diodes connected in series, is partly compensated by the reduced switching losses (which are proportional to the voltage squared of the series connection). Another possibility to reduce the current stress is the use of a current doubler output stage [6,7].

The resulting design leads to an acceptable efficiency and can help to increase the over-all reliability by lowering the component stress.

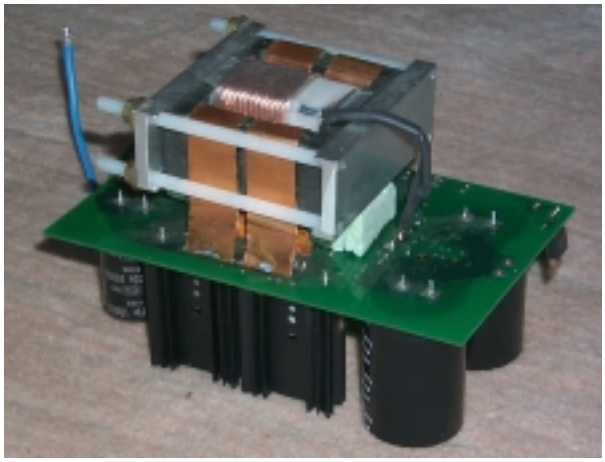

Fig. 13. Breadboarded prototype converter

Figure 13 shows the sample converter. The power transformer was build on one side of the printed circuit board (100 x 160mm), while all electronic components are located on the other one. The resulting design gives advantages in cooling and leads to a satisfactory power density. The design excludes the need of active (fan) cooling up to 1kW. Due to the very low supply of 12V and the resulting high current ratings in this case thick copper traces are necessary (210µm). To avoid voltage overshoots and to minimize the leakage inductances a bifilar layout technique is used.

MEASUREMENT RESULTS

To verify the simulation results a prototype of the proposed converter was breadboard. The inverter operates from a 12V DC-supply. A ETD49 core with N47 material was used. The switching occurred at 330kHz.

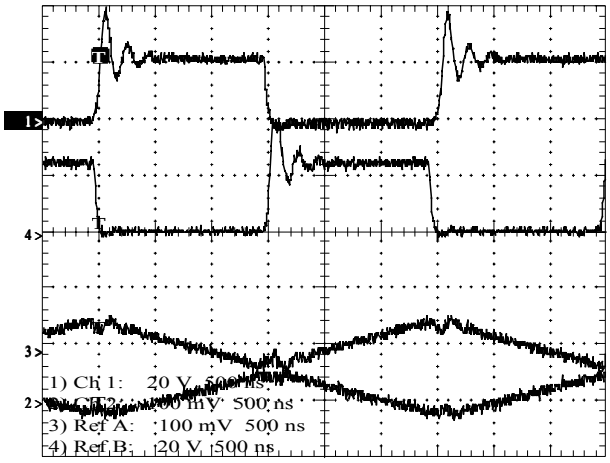

Fig. 14. No load condition, from top to bottom: voltage across switch 1, voltage across switch 2, left side current, right side current

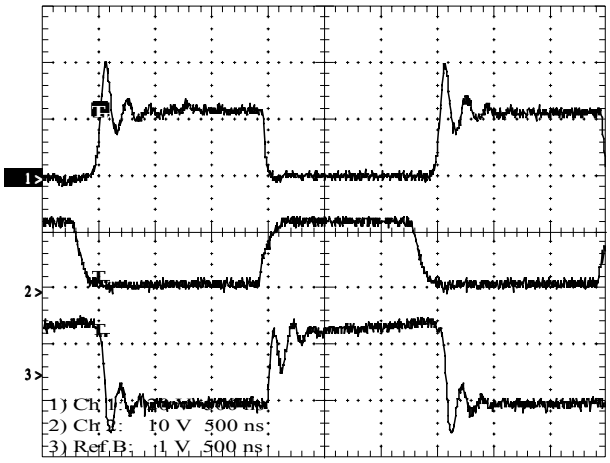

Fig. 15. Full load condition, from top to bottom: voltage across switch 1, gate control signal, current through switch 1 (1V ~ 25A)

Figure 14 shows the converter operating in no-load condition. Contrary to this, in Fig. 15 the sample converter at full load condition is shown. As one can see in Fig. 15 here about 400W are transferred. The over all efficiency of the topology reaches about 97,5%.

Conclusion

The presented converter structure fulfills all requirements of DC-to-DC converters with very low input and high output voltage ratings. The relatively low efficiency which normally occurs due to the high current ratings can be overcome by the magnetic current sharing method eliminating the need of a hard parallel operation of several converter stages to achieve an acceptable total efficiency. The used sharing method is also well suited in most applications, where high current ratings have to be maintained. The breadboard sample converter shows a satisfying efficiency for the usage in solar power applications where high efficiency and an excellent reliability are points of major importance. The chosen design gives advantages in cooling and leads to a satisfactory power density. It excludes the need of active (fan) cooling up to an output power of 1kW.

Due to the rather simple structure, the converter is easy to control. It is well suited for digital implementation in an embedded microcontroller. Modern microcontrollers include most of the peripherals required to implement the full system (ADC, PWM, Timers, etc.). Thus, the solution can be built in a very cheap way, optimal for mass products. On the other hand, the robustness of the design can help to minimize the required computation power, so additional control algorithm can be implemented at the same core (maximum power point tracking, security functions e.g. isolation monitoring on the DC side, mains impedance surveillance to prevent local operation in mains connected applications).

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