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#### Abstract

A fourth order PWM DC/DC or AC/DC converter is treated and a survey over important data (maximum voltage and current ratings for the elements, rms- values for the semiconductor devices and a rough approximation of the losses) of the circuit is given. Furthermore, a converter model including the losses based on duty ratio averaging is established. Due to the bidirectionality of the converter, always continuous inductor current mode occurs. Simulation and measurement results are given.


## I. INTRODUCTION

In the past important work has been done to find new topologies for $\mathrm{DC} / \mathrm{DC}$ conversion [e.g. 1-3]. In [5] twelve fourth order PWM DC/DC converters with limited duty cycle range were treated. By transforming these unidirectional DC/DC converters into bidirectional ones (by shunting the diode with an active switch and the active switch with a diode) converters with interesting DC/DC transfer characteristics can be obtained. One of these possible converter topologies is shown in Fig. 1 and is analyzed in this paper.
A survey over important data (maximum voltage and current ratings for the elements, rms- values for the semiconductor devices and a rough approximation of the losses) of the circuit is given. Furthermore, a dynamic converter model is established. Due to the bidirectionality, the converter works always in the continuous inductor current mode. The losses of the devices are included. Models based on duty ratio averaging are given. A linearized model is also derived as basis for the controller design.


Fig.1. Bidirectional DC-to-AC PWM converter

## II. BASIC ANALYSIS

The basic and idealized shapes of important converter quantities for the stationary, continuous case are given. Figure 2 shows the equivalent circuit of the converter for conducting active switch $S_{1}$ (Fig.2.a) and for conducting active switch $S_{2}$ (Fig.2.b).

Based on the equality of the voltage-timeareas, it is easy to give the transformation relationship for the output voltage $U_{2}$ dependent on the input voltage $U_{1}$ and the duty ratio $d$.
Since for the stationary case the absolute values of the voltage-time areas of the inductors have to be equal, we can easily draw the shapes according to Fig.3. The capacitors are assumed so large that the voltages can be regarded constant during a pulse period. Figure 3 .a shows the current through and the voltage across $\mathrm{L}_{1}$. The current rate of rise of course depends on the values of $\mathrm{L}_{1}$ and $U_{1}$. Figure 3.b shows the current through and the voltage across $L_{2}$. For $L_{1}=L_{2}$ the same current ripple occurs in both inductors. As the voltages are equal across $\mathrm{L}_{1}$ and $\mathrm{L}_{2}$, there exists the possibility to couple the two inductors magnetically and to position them on the same core [4].

2.b

Fig.2. Equivalent circuit of the $\mathrm{DC} / \mathrm{DC}$ converter, a. turn-on switching state, b. turn-off switching


Fig.3.a. Voltage across and current through the inductor $\mathrm{L}_{1}$

From Fig.3.a. we get
$\left(U_{C 1}-U_{1}\right) \cdot d \cdot T=(1-d) \cdot\left(U_{2}+U_{1}\right) \cdot T$
and from Fig.3.b
$U_{2} \cdot d \cdot T=U_{C 1} \cdot(1-d) \cdot T$.
After a few steps we get the voltage transformation law
$U_{C 2}=U_{2}=\frac{1-d}{1-2 d} \cdot U_{1} \quad$ with $\left.d \in\right] 0,1[$.

3.b

Fig.3.b Voltage across and current through the inductor $\mathrm{L}_{2}$


Fig.4. DC voltage transformation factor M in dependence on the duty cycle

Figure 4 shows the voltage transfer ratio $M$ in dependence on the duty cycle. For a duty cycle smaller than 0.5 the converter is a non-inverting step-up converter and for a duty cycle larger than 0.5 it is an inverting step-up/down converter.
Based on the equality of the voltage-time areas in the steady state case, it is easy - as shown above - to get the transformation relationship for the output voltage $U_{2}$ dependent on the input voltage $U_{1}$ and the duty ratio d .

In the same manner a relationship for the currents through the inductors can be derived based on the equality of the absolute values of the current-time-areas of the capacitors during on- and off-times of the active switch $\mathrm{S}_{1}$.


Fig.5.Current through the capacitors C1 (a) and C2 (b)

From Fig.5.a we get for the mean values of the inductor currents $\bar{I}_{L 1}$ and $\bar{I}_{L 2}$
$d \cdot \bar{I}_{L 1}=(1-d) \cdot \bar{I}_{L 2}$.
Obviously, according to Fig. 1 we can write $\bar{I}_{L 1}=\bar{I}_{I N}$.
(The current through the capacitor $C_{2}$ has to be an AC current; otherwise the output voltage would change). The current through $L_{1}$ according to (4) and (5) is

$$
\begin{equation*}
\bar{I}_{L 1}=\bar{I}_{I N}=\frac{1-d}{d} \cdot \bar{I}_{L 2} . \tag{6}
\end{equation*}
$$

Furthermore, it is easy to construct the voltages across and the currents through the active switches (Fig.6) and therefore one can calculate the maximum ratings for the semiconductor devices. It is also important to calculate the relationship between the input current, the load current, and the currents through the inductors to get dimensioning information for the thermal and magnetic design.
$\bar{I}_{L 1}=\frac{1-d}{1-2 \cdot d} \cdot I_{\text {Load }}$
$\bar{I}_{L 2}=\frac{d}{1-2 \cdot d} \cdot I_{\text {Load }}$.
From the equivalent circuits one can immediately see that the current through the semiconductor devices is the sum of the inductor currents (through the switch $\mathrm{S}_{1}$ during $\mathrm{T}_{\text {on }}$, through the switch $\mathrm{S}_{2}$ during $\mathrm{T}_{\text {off }}$ ). Therefore, the
current maximum values for the semiconductor devices are

$$
\begin{equation*}
I_{D S 1, \max }=I_{D S 2, \max }=\left(\hat{I}_{L 1}+\hat{I}_{L 2}\right) . \tag{8}
\end{equation*}
$$

For the calculation of the on-state losses the rms values are important. For the active switches $S_{1}$ and $S_{2}$ we get approximately (the current ripple is omitted)

$$
\begin{aligned}
& I_{D S 1, r m s}=\frac{I_{\text {load }}}{1-2 d} \cdot \sqrt{d} \\
& I_{D S 2, r m s}=\frac{I_{\text {load }}}{1-2 d} \cdot \sqrt{1-d} . \\
& \\
& \\
& \\
& \mathrm{u}_{\mathrm{DS} 1} \uparrow \\
&
\end{aligned}
$$

a.

b.

Fig.6. Voltage across and current through the semiconductor devices, a. active switch, b. passive switch

Figure 6 shows the current through the active switch $\mathrm{S}_{2}$ (Fig.6.b) and the active switch $S_{1}$ (Fig.6.a) Due to the input inductor, a relatively constant current is taken from the voltage source.
For the dimensioning of the circuit, the voltage rates for the semiconductors are important. According to the equivalent circuit for the on-state ( $\mathrm{S}_{1}$ on, $\mathrm{S}_{2}$ off, Fig.2.a) the voltage across $S_{2}$ is
$U_{D S 2, \text { max }}=U_{1}+U_{C 1}=U_{1} \cdot \frac{1}{d}$
and according to Fig.2.b ( $\mathrm{S}_{1}$ off, $\mathrm{S}_{2}$ on) the voltage across switch $S_{1}$ is
$U_{D S 1, \max }=U_{1}+U_{C 1}=U_{1} \cdot \frac{1}{d}$
The voltage ratings for the semiconductor devices are indirectly proportional to the duty cycle. Figure 6 shows this relation graphically.
For continuous operation-mode and synchronous rectification, which are used in principal in this converter topology, it is easy to calculate a rough approximation of the efficiency of the converter. With $r_{D S}$ as on-resistance of the semiconductors we can calculate the conduction losses (without switching losses) according to
$P_{V} \approx r_{\text {DSon }} \cdot \frac{I_{\text {load }}{ }^{2}}{(1-2 d)^{2}}$
and further get a rough estimate of the efficiency with the equation
$\eta=\frac{\left(U_{2} \cdot I_{\text {load }}\right)}{\left(U_{2} \cdot I_{\text {load }}\right)+P_{V}}$.
An interesting aspect of the circuit is given by the fact that the voltage is equal across both inductors. This makes possible a coupling of $\mathrm{L}_{1}$ and $\mathrm{L}_{2}$ and therefore to have only one magnetic part in the circuit (integrated magnetics).

## III. MODEL REPRESENTATION

For the sake of brevity the consideration of the following details shall be omitted: the influence of the ESR (equivalent series resistance) of the capacitors and of the ohmic contribution of the inductive storage elements on the control behavior; also ideal switches are assumed. However, only a model with loss resistances gives good consistency with practical experiments. It is given in (20) at the end of part III. As the converter is always in the continuous mode of operation, one can establish two describing differential equation systems for closed active switch S1 (and therefore open switch S2) and for open switch S1 (and therefore closed switch S2) respectively. These two systems can be combined into one system of differential equations. Then this system of nonlinear differential equations can be linearized around its operating point enabling the use of the linear control theory. During the interval $\mathrm{T}_{\mathrm{on}}$ (with reference to switch S1), the equivalent circuit of Fig.2.a is valid, leading to the equations
$\frac{d i_{L 1}}{d t}=\frac{-u_{1}+u_{C 1}}{L_{1}}$
$\frac{d i_{L 2}}{d t}=\frac{u_{C 2}}{L_{2}}$
$\frac{d u_{C 1}}{d t}=\frac{-i_{L 1}}{C_{1}}$
$\frac{d u_{C 2}}{d t}=\frac{-i_{L 2}-\left(u_{C 2} / R\right)}{C_{2}}$.
During the interval $\mathrm{T}_{\text {off }}$ the equivalent circuit of Fig.2.b is valid; the corresponding equations are
$\frac{d i_{L 1}}{d t}=\frac{-u_{C 2}-u_{1}}{L_{1}}$
$\frac{d i_{L 2}}{d t}=\frac{-u_{C 1}}{L_{2}}$
$\frac{d u_{C 1}}{d t}=\frac{i_{L 2}}{C_{1}}$
$\frac{d u_{C 2}}{d t}=\frac{i_{L 1}-u_{C 2} / R}{C_{2}}$.
(14) and (15) describe the system behavior. Under the condition that the system time constants are large compared to the switching period, we can combine these two sets of equations. The duty ratio shall be defined as $d=\frac{T_{\text {on }}}{T}$.
Weighed by this duty ratio, the combination of the two sets yields

$$
\frac{d}{d t}\left(\begin{array}{c}
i_{L 1}  \tag{17}\\
i_{L 2} \\
u_{C 1} \\
u_{C 2}
\end{array}\right)=\left[\begin{array}{cccc}
0 & 0 & \frac{d}{L_{1}} & -\frac{1-d}{L_{1}} \\
0 & 0 & -\frac{1-d}{L_{2}} & \frac{d}{L_{2}} \\
-\frac{d}{C_{1}} & \frac{1-d}{C_{1}} & 0 & 0 \\
\frac{1-d}{C_{2}} & \frac{-d}{C_{2}} & 0 & -\frac{1}{R \cdot C_{2}}
\end{array}\right] \cdot\left(\begin{array}{c}
i_{L 1} \\
i_{L 2} \\
u_{C 1} \\
u_{C 2}
\end{array}\right)+\left(\begin{array}{c}
-\frac{1}{L_{1}} \\
-\frac{1-d}{L_{2}} \\
0 \\
0
\end{array}\right) \cdot u_{1}
$$

By the given system of equations, the dynamic behavior of the idealized converter is described correctly in the average; thus quickly giving us a general view of the

$$
\frac{d}{d t}\left(\begin{array}{l}
\hat{i}_{L 1}  \tag{19}\\
\hat{i}_{L 2} \\
\hat{u}_{C 1} \\
\hat{u}_{C 2}
\end{array}\right)=\left[\begin{array}{cccc}
0 & 0 & \frac{D_{0}}{L_{1}} & \frac{D_{0-1}}{L_{1}} \\
0 & 0 & \frac{D_{0}-1}{L_{2}} & \frac{D_{0}}{L_{2}} \\
-\frac{D_{0}}{C_{1}} & \frac{1-D_{0}}{C_{1}} & 0 & 0 \\
\frac{1-D_{0}}{C_{2}} & -\frac{D_{0}}{C_{2}} & 0 & -\frac{1}{C_{2} \cdot R}
\end{array}\right] \cdot\left(\begin{array}{cc}
\hat{i}_{L 1} \\
\hat{i}_{L 2} \\
\hat{u}_{C 1} \\
\hat{u}_{C 2}
\end{array}\right)+\left[\begin{array}{cc}
-\frac{1}{L_{1}} & \frac{U_{C 10}+U_{C 20}}{L_{1}} \\
\frac{D_{0}}{L_{2}} & \frac{U_{C 10}+U_{C 20}}{L_{2}} \\
0 & -\frac{I_{L 10}+I_{L 20}}{C_{1}} \\
0 & -\frac{I_{L 10}+I_{L 20}}{C_{2}}
\end{array}\right] \cdot\binom{\hat{u}_{1}}{\hat{d}}
$$

and the model with included parasitic resistances is

$$
\frac{d}{d t}\left(\begin{array}{l}
i_{L 1}  \tag{20}\\
i_{L 2} \\
u_{C 1} \\
u_{C 2}
\end{array}\right)=\left[\begin{array}{cccc}
-\frac{r_{D S}+r_{L 1}+d \cdot r_{C 1}+\left(R_{L} / / r C 2\right) \cdot(1-d)}{L_{1}} & -\frac{r_{D S}}{L_{1}} & \frac{d}{L_{1}} & \frac{(d-1) \cdot R_{L}}{\left(R_{L}+r_{C 2}\right) \cdot L_{1}} \\
-\frac{r_{D S}}{L_{2}} & -\frac{r_{D S}+r_{L 2}+\left(r_{C 2} / / R_{L}\right) \cdot d+r_{C 1} \cdot(1-d)}{L_{2}} & \frac{d-1}{L_{2}} & \frac{d \cdot R_{L}}{L_{2} \cdot\left(R_{L+}+r_{C 2}\right)} \\
-\frac{d}{C_{1}} & \frac{1-d}{C_{1}} & 0 & 0 \\
\frac{(1-d) \cdot R_{L}}{\left(r c 2+R_{L}\right) \cdot C_{2}} & -\frac{d \cdot R_{L}}{\left(r_{C 2}+R_{L}\right) \cdot C_{2}} & 0 & -\frac{1}{\left(r_{C 2}+R_{L}\right) \cdot C_{2}}
\end{array}\right] \cdot\left(\begin{array}{c}
i_{L 1} \\
i_{L 2} \\
u_{C 1} \\
u_{C 2}
\end{array}\right)+\left(\begin{array}{c}
\frac{d}{L_{1}} \\
\frac{1-d}{L_{2}} \\
0 \\
0
\end{array}\right) \cdot u_{1}
$$

## IV. SIMULATION AND MEASUREMENTS

The voltage transfer ration (Fig.4) shows a singularity at $\mathrm{d}=0.5$. Inspection of Fig. 1 reveals that the polarity of the input voltage has to be changed, when the duty cycle exceeds 0.5 . The output voltage is always in the same direction. It is therefore obvious that the converter can direction. It is therefore obvious that the converter can
also be used as a rectifier. Figures 7,8 depict the output voltage during start-up of the converter, when a sinusoidal input voltage
dynamic behavior of the converter. The superimposed ripple (which appears very pronounced in the coils) is of no importance for qualifying the dynamic behavior. The voltage ripple across the capacitors is very small anyhow in SMPS (switched mode power supply) where a smooth DC voltage is of importance. This is due to the sufficiently large dimensioning of the capacitors. This model is also appropriate as large-signal model because no limitations with respect to the signal values have been made. The weighed matrix differential equation (17) representing the dynamic behavior of the converter is a nonlinear one. To use the possibilities of linear control theory, a linearization is necessary. With capital letters for the operating point values and small letters for the disturbance around the operating point
$i_{L 1}=I_{L 10}+\hat{i}_{L 1}$
$i_{L 2}=I_{L 20}+\hat{i}_{L 2}$
$u_{C 1}=U_{C 10}+\hat{u}_{C 1}$
$u_{C 2}=U_{C 20}+\hat{u}_{C 2}$
$u_{1}=U_{C 10}+\hat{u}_{1}$
$d=D_{0}+\hat{d}$
one can calculate the linearized model of the converter according to
$u_{1}=\hat{U}_{1} \cdot \sin \omega t$
of different frequencies $(50 \mathrm{~Hz}, 400 \mathrm{~Hz})$ is applied. The modulation function

$$
\begin{equation*}
d=\frac{U_{2}-\hat{U}_{1} \cdot \sin \omega t}{2 \cdot U_{2}-\hat{U}_{1} \cdot \sin \omega t} \tag{22}
\end{equation*}
$$

is necessary to achieve the desired voltage $U_{2}$ across the output capacitor $C_{2}$. Pulse width modulation of this duty cycle function leads to the necessary gate signals of the
active switches. The simulation was done with model (20).


Fig.7.a. Output voltage during start-up in rectifier mode


Fig.7.b. Input voltage and output voltage during start-up in rectifier-mode, input frequency 50 Hz (AC/DC mode)


Fig.8. Output voltage during start-up in rectifier-mode, input frequency 400 Hz (AC/DC mode)

In Fig. 9 start-up and step-response of the output voltage due to a step in the duty cycle are presented. The converter works in the non-inverting boost-mood. The smooth curve during start-up is because of the lack of a current limitation. In Fig. 10 start-up and step-response of the output voltage due to a step in the duty cycle for a converter in the inverting buck-boost mode are shown. Once more the smooth curve during start-up is because of the lack of a current limitation.


Fig.9. Start-up and duty cycle step from $\mathrm{d}=0.30$ to 0.35 , DC/DC mode


Fig.10. Start-up and duty cycle step from d=0.65 to 0.7, DC/DC mode

The following results prove the derived theory and show the functionality of the proposed converter. To achieve a controlled output voltage, the duty cycle has to be modulated. Figure 11 shows the DC conversion ratio M, (the ratio of output to input voltage) of a small model converter.


Fig.11. DC voltage transformation rate $M=U_{2} / U_{1}$ $U_{1}=24 \mathrm{~V}$

Figures 12,13 show the currents through the two converter inductors $L_{1}$ and $L_{2}$ for a duty cycle of $80 \%$ and $30 \%$ respectively. The current rate of rise is the same in both inductors. Due to the relatively small switching frequency, a relativly large current ripple occurs.


Fig.12. Current through the two inductors 2A/div d=30\%, upper trace current through $\mathrm{L}_{1}$ and lower trace current through $\mathrm{L}_{2}$

In Figs. 13 and 14 a step-response of the output voltage due to a step in the duty cycle is presented. There is no over-shot.


Fig.13. Response of the output voltage due to a $20 \%$ to $30 \%$ duty cycle step


Fig.14. Response of the output voltage due to a $70 \%$ to $60 \%$ duty cycle step

## V. CONCLUSIONS

A bidirectional converter, which enables to useboth voltage directions on the input, was investigated. For the capacitor C2, which buffers the output voltage, an electrolyte capacitor can be used. An interesting aspect of the circuit is given by the fact that the voltage is equal across both inductors. This makes possible a coupling of the two inductors on one common core leading to only one magnetic device in the circuit. A further advantage of the converter is a constant current drawn from the source. The converter can be used as an AC-to-DC converter with power factor correcting ability. In this case a feed forward control with a superimposed feedback, which corrects the errors which are not modeled correctly by the control law (e.g. changes and deviations of the parasitic elements), would be adviseable. The converter can also be used as a two quadrant driver for DC machines working from an AC mains.

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