AN ISOLATED DC-DC CONVERTER WITH +/-220V BALANCED OUTPUTS FOR TELECOM SYSTEMS

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Abstract. This work proposes a new strategy to improve the double-output DC-to-DC converter. The isolated full-bridge topology is zero-voltage switched (ZVS) and the pulse-width modulation is phase-shifted (PS-PWM). The high-frequency isolation transformer has two secondary windings to feed both the +220V and –220V DC outputs. The output filtering inductors are coupled together to balance the output voltages. A very simple command circuit, using only one integrated circuit, is employed to obtain regulated DC outputs and to drive the switches.

INTRODUCTION

It is great the search for more reliable power supply to Telecommunications Systems for both, DC and AC systems. The DC system is used in several voltage levels for consumers and battery charger connected in the AC line, the DC system is also required to supply AC voltage used in uninterruptible power systems (UPS), through the accumulation batteries, when some fault in the mains happens.

In this context, the purpose of this work is to present a very robust choice for the input stage of an inverter circuit. The converter used in this DC-DC stage should attend to following demands:

- The input source uses a 72V battery bank, with a voltage variation range from 60 up to 90V;
- Two symmetrical and regulated DC outputs with voltages of +220V and –220V, with low ripple;
- Isolation between the input and the output;
- The load is non-linear type - it supplies a 1.5kVA half-bridge inverter circuit.

The converter topology chosen for this task was the full-bridge converter, which makes possible the high-frequency isolation at this power level, with excellent utilization of the transformer. Besides, the command strategy is very simple, it uses the phase-shifted pulse-width modulation (PS-PWM) and it is also obtained zero-voltage switching (ZVS) for all of the main switches, Andreycak (1) and Heldwein (2).

The proposed converter presents high efficiency due to the near zero commutation losses and reduced conduction losses due to the current-mode output characteristics. This topology also presents reduced levels of electromagnetic interference, for conducted and irradiated noises, due to the soft-switching technique. Another great advantage of this converter is using the leakage inductance of the transformer and the output capacitance of the switches to allow soft switching. In other words, instead of these elements being a worrying trouble, they can be used in benefit to the performance of the converter.

FULL-BRIDGE CONVERTER

The basic topology of the proposed converter, with symmetrical DC outputs, is shown in Fig. 1.

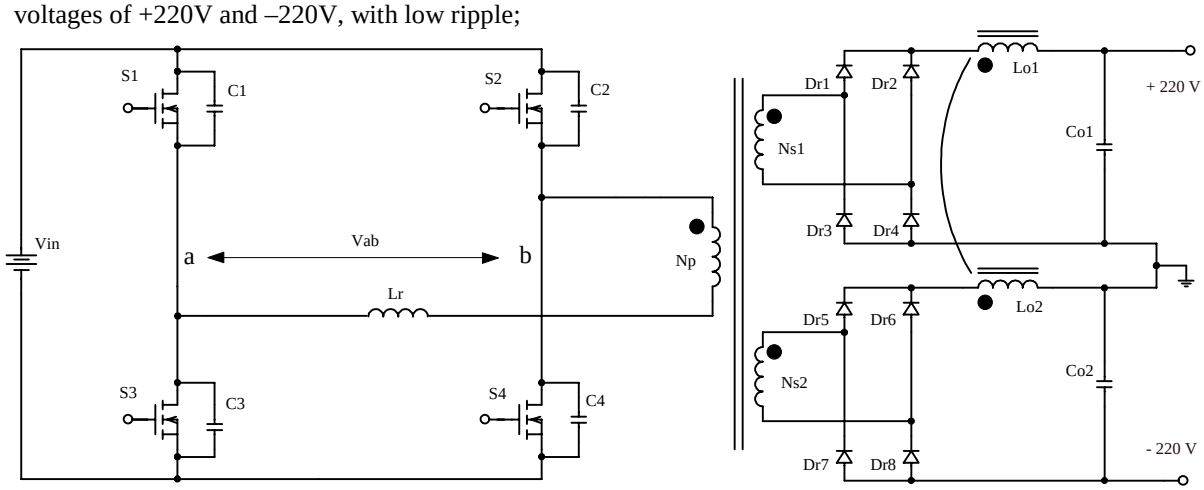

Figure 1: full-bridge converter with symmetrical DC outputs.

Operation stages

For the operation analysis of this topology, the two DC outputs can be considered as only one DC output connected through only one secondary winding. Besides, the following simplifications are adopted:

- All of the circuit components are considered ideals;
- The capacitor used to block the DC components, placed in series with the primary winding, is considered as a short-circuit in the switching frequency;
- Each inductor of the output filters is considered as a current-source and this current is referred to the primary side of the transformer.

1st stage: (t_0 - t_1) - Fig. 2. In t_o, when the voltage across capacitor C_1 goes to zero, the diode D_1 is biased and it is turned on. During this stage the current I_o' stays freewheeling through the rectifier diodes and the resonant inductor current stays freewheeling through S_2 and D_1.

2nd stage: (t_1 - t_2) - Fig. 3. At t_1 the switch S_2 is turned off. The voltages across capacitors C_2 and C_4 and the current in the resonant inductor evolve resonantly. This stage ends when the voltage on C_4 goes to zero.

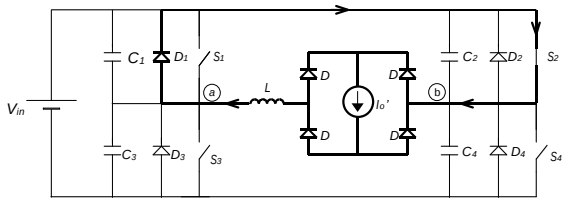

Figure 2: First stage.

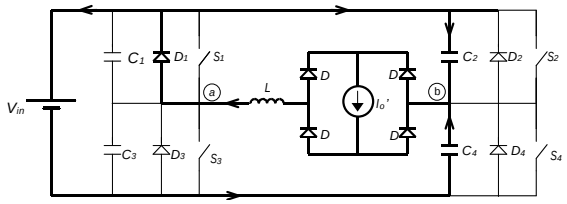

Figure 3: Second stage.

3rd stage: (t_2 - t_3) – Fig. 4. At t_2, the voltage across C_4 equals zero, the diode D_4 is biased and begins to conduct. The current through resonant inductor decreases lineally until it reaches zero. The switch S_4 should be enabled during this stage.

4th stage: (t_3 - t_4) – Fig. 5. At t_3, the resonant inductor current changes its direction and circulates through switches S_1 and S_4. Thereafter, this current grows linearly until it reaches the value of the output current I_o'.

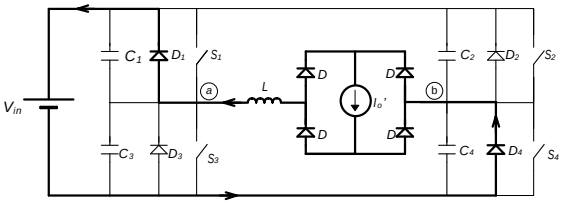

Figure 4: Third stage.

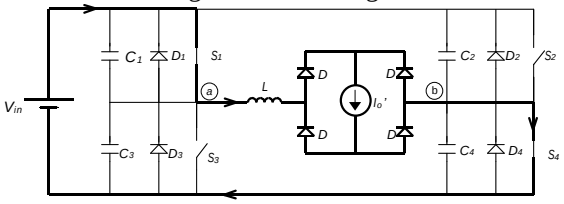

Figure 5: Fourth stage.

5th stage: (t_4 - t_5) – Fig. 6. In this stage occurs the transference of energy from the input source to the load, through S_1 and S_4.

6th stage: (t_5 - t_6) – Fig. 7. At t_5, the switch S_1 is turned off. The voltages across C_1 and C_3 and the resonant inductor current evolve resonantly. This stage ends when the voltage on C_3 goes to zero.

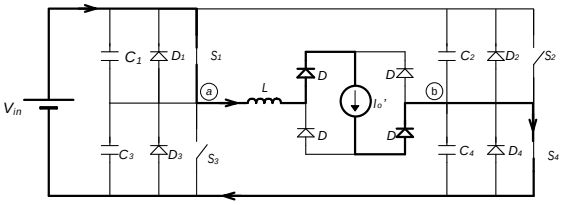

Figure 6: Fifth stage.

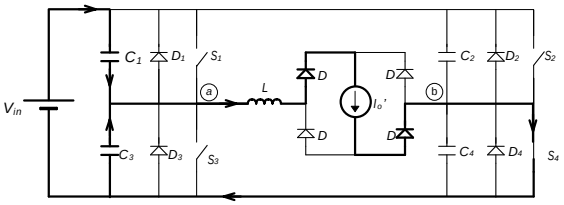

Figure 7: Sixth stage.

7th stage: (t_6 - t_7) – Fig. 8. In t_6, when the voltage in the capacitor C_3 goes to zero, the diode D_3 is biased and begins to conduct. During this stage the current I_o' stays freewheeling through the rectifier diodes and the resonant inductor current stays freewheeling through S_4 and D_3.

8th stage: (t_7 - t_8) – Fig. 9. At t_7, the switch S_4 is turned off and the voltages across capacitors C_2 and C_4 and the inductor current evolve resonantly. This stage ends when the voltage across C_2 goes to zero.

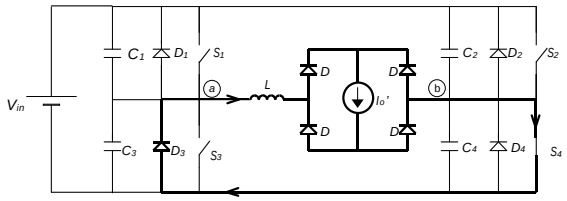

Figure 8: Seventh stage.

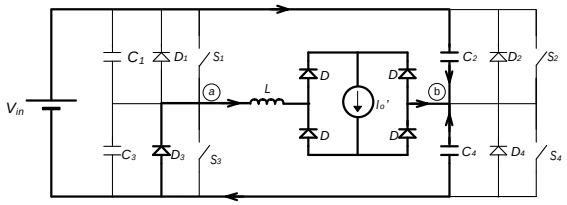

Figure 9: Eighth stage.

9th stage: (t_8 - t_9) – Fig. 10. At t_8, when the voltage across capacitor C_2 goes to zero, the diode D_2 is biased and begins to conduct. The current through the resonant inductor decreases lineally until it is annulling. The switch S_2 should be enabled during this stage.

10th stage: (t_9 - t_{10}) – Fig. 11. In t_9, the current in the resonant inductor changes its direction and circulates through switches S_2 and S_3. Thereafter, this current grows lineally until it reaches the value of the output current I_o'.

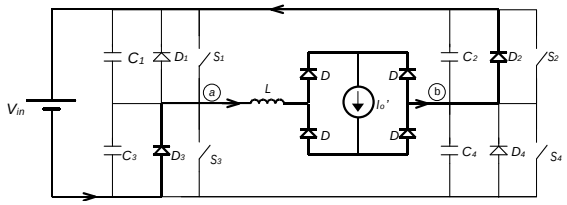

Figure 10: Ninth stage.

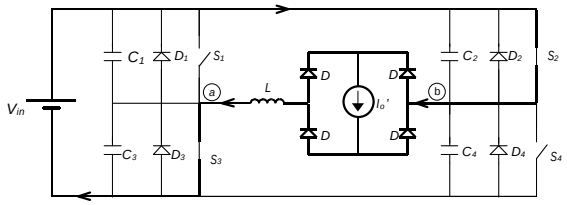

Figure 11:Tenth stage.

11th stage: (t_{10} - t_{11}) – Fig. 12. In this stage occurs the transference of energy from the input source to the load, through S_2 and S_3.

12th stage: (t_{11} - t_{12}) – Fig. 13. In t_{11}, the switch S_3 is turned off and the voltages across capacitors C_1 and C_3 and the resonant inductor current evolve resonantly. This stage ends when the voltage across C_1 reaches zero.

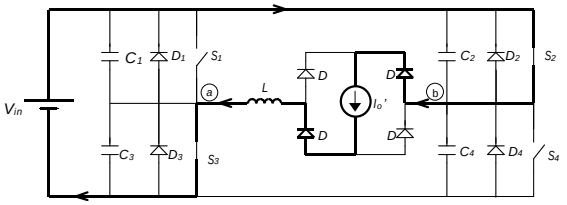

Figure 12: Eleventh stage.

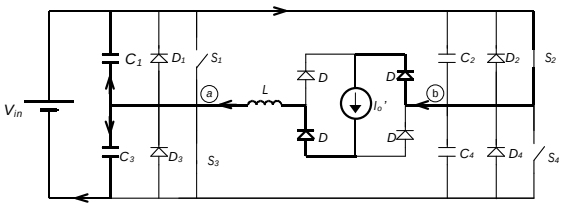

Figure 13: Twelfth stage.

Main waveforms

The most relevant waveforms, described for each operation stage, are shown in Fig. 14.

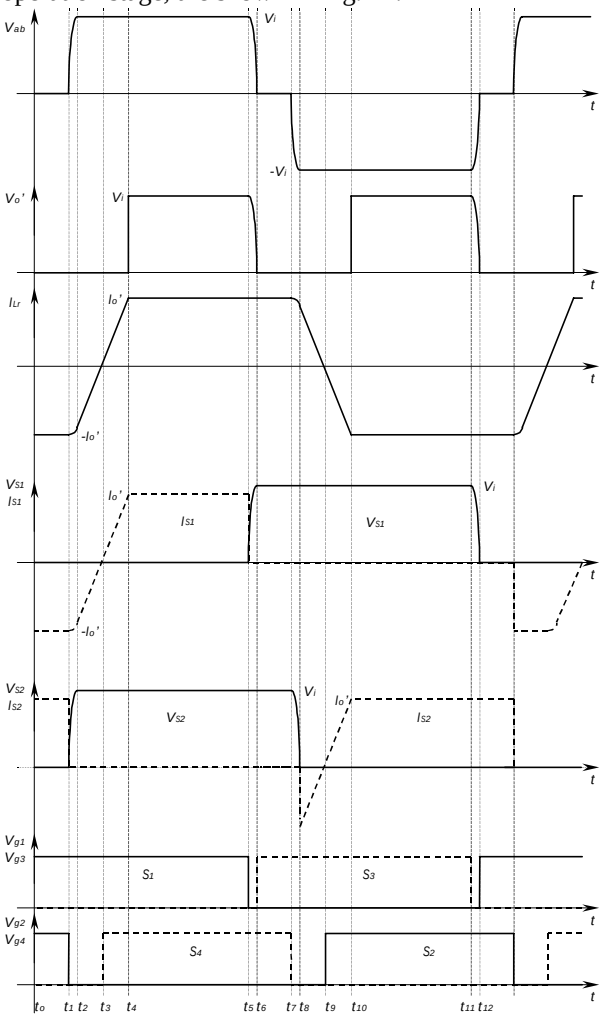

Figure 14: Main waveforms.

Output characteristic

Since the current in the resonant inductor evolves lineally, as observed in stages 3rd, 4th, 9th and 10th, the load is short-circuited by the diode rectifier. Only on the 5th and the 11th stages happens energy transference from supply to load. Therefore, it becomes possible to define an effective duty cycle (D_{ef}) as the time where energy transference happens.

Fig. 15 shows the voltage and the current between the points (a) and (b) during half switching cycle.

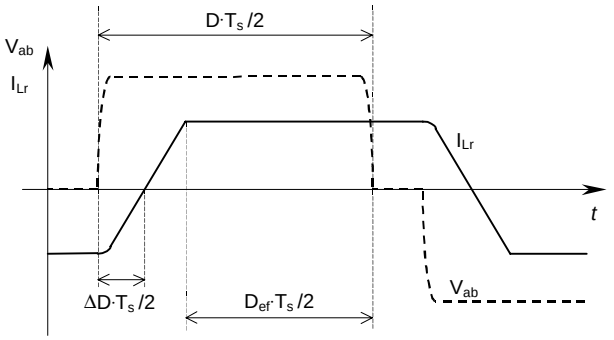

Figure 15: Voltage and current between the points (a) and (b)

From the analysis of the circuit and Fig. 15, the following equation can be written:

$$V_{in} = L_r \cdot \frac{2 \cdot I_o^{'}}{\Delta t} \cdot \frac{N_s}{N_p} \quad (1)$$

Where:

$$\Delta t = \Delta D \cdot \frac{T_s}{2} \quad (2)$$

The conventional full-bridge converter presents the following characteristic:

$$V_o = V_{in} \cdot D_{ef} \cdot \frac{N_s}{N_p} \quad (3)$$

The effective duty cycle is defined as:

$$D_{ef} = D - \Delta D \quad (4)$$

From (1), (2) and (3), the equation for the output characteristic results:

$$\frac{V_o}{V_{in}} = \frac{N_s}{N_p} \cdot \left(D - \frac{4 \cdot f_s \cdot L_r \cdot I_o^{'}}{V_i} \cdot \frac{N_s}{N_p} \right) \quad (5)$$

Analysis of the transitions

Transition current is responsible to charge and discharge the capacitors placed in parallel with the switches (added to the output capacitance of the switches). When the operation stages is observed, it is verified that the left leg, composed by the switches S_1 and S_3, has the transition current equal to the load current I_o'. On the other hand, the right leg, composed by S_2 and S_4, always commute with a lower current, because the diode rectifiers are short-circuited during this transition. In this way, the transition of the right leg does not happen in such favorable conditions as the left leg. In lower load operation (smaller currents), soft commutation condition can be missed.

Right leg transition

The commutations in this leg happen with the diode rectifiers short-circuited, as shown in second and eighth operation stages. Therefore, there is only the stored energy in the resonant inductor to accomplish these commutations.

During this leg transition, a minimum current in the resonant inductor should be guaranteed. So, enough energy is necessary to accomplish soft commutation.

To guarantee soft commutation for a wide load, the inductance value of the resonant inductor should be increased. However, the effective duty cycle decreases as the inductance of the resonant inductor increases. In fact, there is a trade-off between soft commutation and duty cycle loss.

Left leg transition

In this leg, the load current I_o' helps the transition, as shown in the sixth and tenth stages. Therefore, this transition is less critical than the right-leg one.

DESIGN AND SPECIFICATION OF THE CIRCUIT COMPONENTS

The proposed topology is presented in Fig. 16. The diodes D_{s1} and D_{s2} are used to clamp the over-voltage across the switches due to the reverse recovery effects of the output diodes, Redl et al (3).

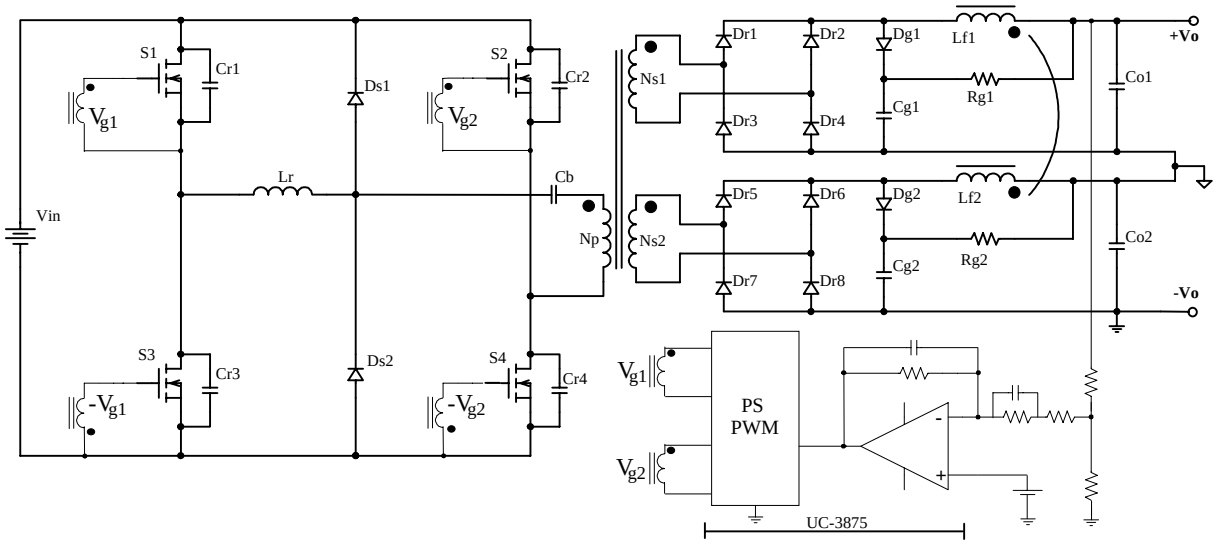

Figure 16: Complete circuit of the proposed converter.

The balanced voltage of the two outputs is guaranteed by magnetic coupling between the two inductors of the output filters, Bascopé and Barbi (4). This solution uses the power circuit characteristics, together with the presented coupling strategy to accomplish this balance. Usually, this balance has been reached through a more complex command and control strategy.

Fig. 17 shows the circuit used to analyze the magnetic coupling of the two output inductors. The diode rectifiers and the secondary windings are replaced by two AC voltage sources at a magnitude corresponding to the AC ripple of the rectified voltage. Thus, the following equations are obtained:

$$V_1 = L_{f1} \cdot \frac{dI_1}{dt} + M \cdot \frac{dI_2}{dt} + V_{c1} \quad (6)$$

$$V_2 = L_{f2} \cdot \frac{dI_2}{dt} + M \cdot \frac{dI_1}{dt} + V_{c2} \quad (7)$$

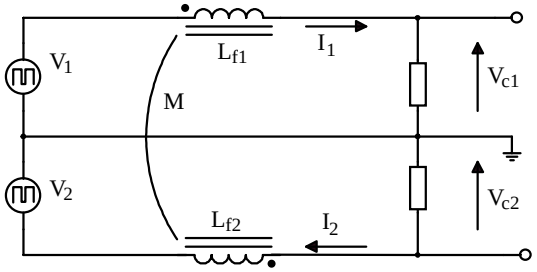

Figure 17: Simplified circuit used to analyze the magnetic coupling of the output inductors.

Considerations:

- The output inductances are the same ($L_{f1}=L_{f2}=L_f$);
- The leakage inductance is negligible ($L_f = M$);
- The rectified voltages are the same ($V_1 = V_2 = V$).

From equations (6) and (7) we can get:

$$V_{c1} = V - L_f \cdot \frac{dI_1}{dt} - L_f \cdot \frac{dI_2}{dt} \quad (8)$$

$$V_{c2} = V - L_f \cdot \frac{dI_2}{dt} - L_f \cdot \frac{dI_1}{dt} \quad (9)$$

Considering unbalance of the loads ($I_1 \neq I_2$), the output voltages are equals ($V_{c1}=V_{c2}$).

When the loads are balanced ($I_1 = I_2 = I$). The equivalent circuits, for the output inductors designed without and with magnetic coupling, are shown in Figs. 18 and 19, respectively.

From the analysis of the circuit without coupling, the following equation is obtained:

$$2 \cdot V = 2 \cdot L_f \cdot \frac{dI}{dt} + 2 \cdot V_c \quad (10)$$

From analysis of the circuit with coupling between the inductors, the following equation is obtained:

$$2 \cdot V = 4 \cdot L_{coup} \cdot \frac{dI}{dt} + 2 \cdot V_c \quad (11)$$

From the equations (10) and (11) it is observed that, for the coupling circuit (Fig. 19) to reproduce the same current ripple of the circuit without magnetic coupling (Fig. 18), the necessary inductance is a half of that used in the circuit without coupling.

$$L_{coup} = \frac{L_f}{2} \quad (12)$$

To allow regulation of the DC output, the voltage regulator, internal component of the IC, receives a sample of the total voltage of the two DC outputs and it compares with a reference voltage. The error signal goes into the PS-PWM to generate the pulses to drive the switches through two pulse transformers.

The full-bridge converter uses the resonant elements L_r and C_{r1} to C_{r4} to obtain soft commutation (ZVS) in the switches. The diodes D_{s1} and D_{s2} help to clamp the over-voltage on the switches. To avoid over-voltages due to the leakage inductance of the transformer and the leakage inductance of the coupled inductors, a low-loss snubber circuit is placed in each output. Thus, high reliability and robustness is also ensured.

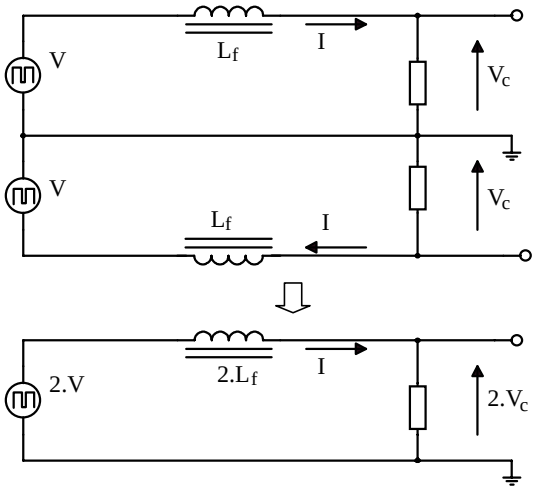

Figure 18: Equivalent circuit for two separately winding up inductors.

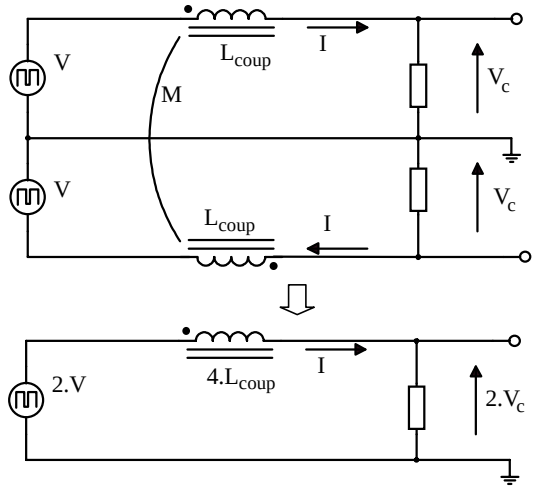

Figure 19: Equivalent circuit for magnetically coupled inductors.

Specifications and relevant components

- Output power P_o = 1.5kW
- Output voltages V_o = (+220V and -220V)
- Input voltage V_{in} = 72 V (60 up to 90V)
- Switching frequency f_s = 70 kHz
- Transformer
  Ferrite core = EE-65/39
  N_p = 5 turns with 66 x 25AWG wires
  N_{s1} = 23 turns with 8 x 25AWG wires
  N_{s2} = 23 turns with 8 x 25AWG wires
- Resonant inductor:
  L_r = 1µH
  Ferrite core = EE-42/15
  N_{Lr} = 2 turns with 66 x 25AWG wires
- Resonant capacitors:
  C_1 to C_4 = 33µF
- Main switches:
  S_1 to S_4 = 2 x IRFP260 (IR) (parallel connected).
  Losses = 128W
- DC-blocked capacitor:
  C_b = 47µF
- Inductor of the output filter:
  $L_{f1} = L_{f2}$ = 1.3 mH
  L_{coup} = 650µH
  Ferrite core = EE-55/21
  L_{f1} = 48 turns with 5 x 25AWG wires
  L_{f2} = 48 turns with 5 x 25AWG wires
- Rectifiers diodes:
  D_{r1} to D_{r8}: MUR860 (Motorola)
- Snubber circuits:
  $D_{g1} = D_{g2}$ = MUR160
  $C_{g1} = C_{g2}$ = 100µF / 600V
  $R_{g1} = R_{g2}$ = 20k Ω / 5W

EXPERIMENTAL RESULTS

Nominal and balanced load

The experimental results for operation with nominal load for both outputs are presented. Fig. 20 shows the waveforms of the voltage between the points (a) and (b) of the power circuit and the current through one secondary winding. Fig. 21 shows the current waveforms through output inductors.

The waveform of the voltage on the DC-blocking capacitor, connected in series with the primary winding of the transformer, is shown in Fig. 22.

Unbalanced load

When the converter operates with unbalanced load, the magnitudes of the output voltages stay practically equal (near 220V). This voltage balance is due to the magnetic coupling of the inductors. Fig. 23 shows the current waveforms through output inductors when one of the outputs operates with nominal load and the other one, reduced to 50% of the nominal load.

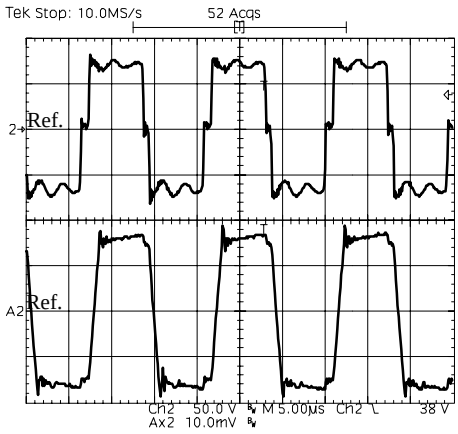

Figure 20: V_{ab} and current in a secondary winding (50V/div, 1A/div and 5µs/div).

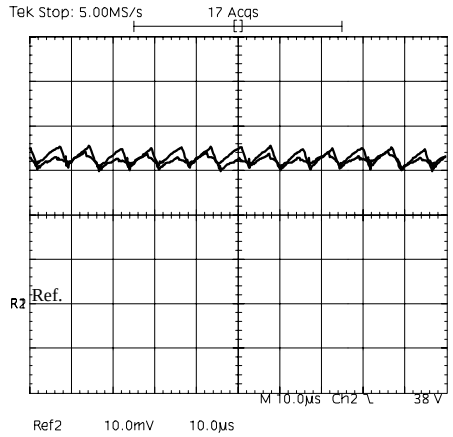

Figure 21: Currents through output inductors (1A/div and 10µs/div).

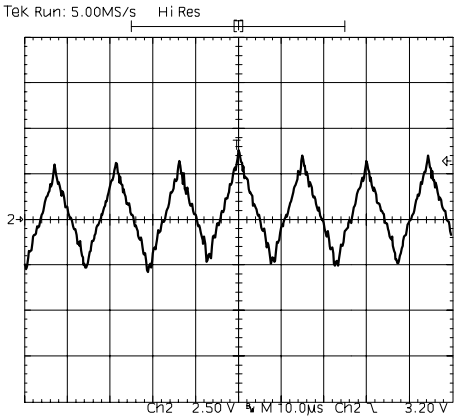

Figure 22: Voltage on the DC-blocked capacitor (2,5V/div and 10µs/div).

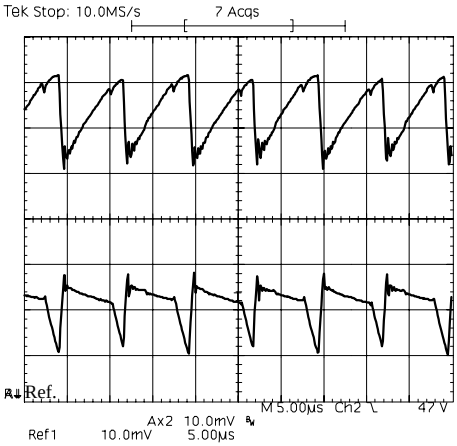

Figure 23: Currents in the coupled inductors (0.5A/div and 5µs/div)

Load transient

In this experiment, one of the loads is maintained in the nominal value and the other is turned on and turned off. The waveforms of the current through load, which is being switched, and the total voltage (ripple) on the outputs, are shown in Figs. 24 and 25, respectively. One of the loads is turned on and later turned off.

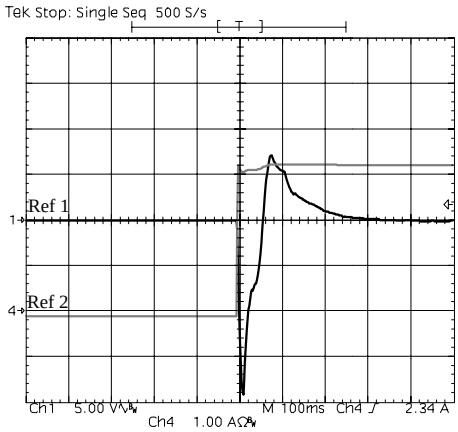

Figure 24: Current through load and output voltage (5V/div, 1A/div and 100ms/div) – turn on

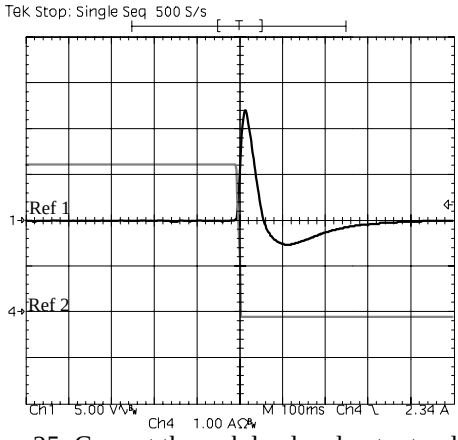

Figure 25: Current through load and output voltage (5V/div, 1A/div and 100ms/div)– turn off

Voltage regulation

In this experiment, one output (1) is maintained with nominal load and the other output (2) rises from zero to full load. Fig. 26 shows the two output voltages versus the current through the output 2.

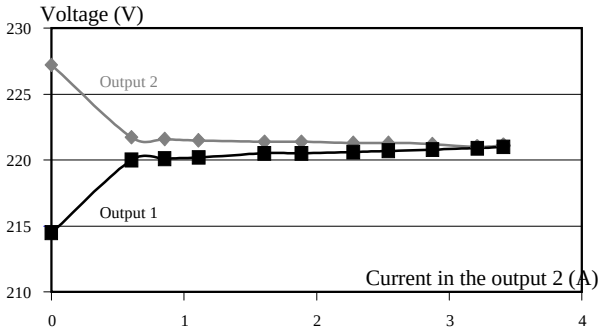

Fig. 26: Voltages on the two outputs versus current in one output.

Efficiency

The efficiency curve, obtained for balanced loads, is shown in Fig. 27.

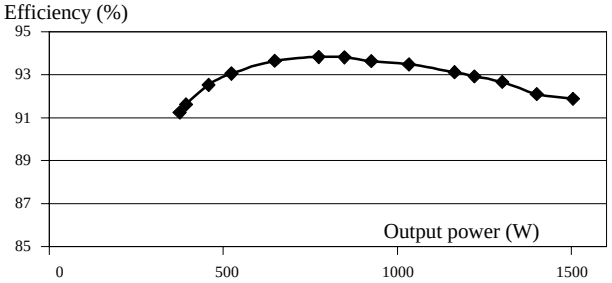

Figure 27: Efficiency.

CONCLUSIONS

This work presented a 1.5kW DC-to-DC step-up converter, with symmetrical outputs, to be used as an input stage of a half-bridge inverter. The topology used was the isolated full-bridge converter, with phase-shifted pulse width modulation (PS-PWM). In the power stage, the switches were commuted with zero voltage (ZVS), ensured by a resonant circuit.

The two symmetrical DC outputs of +220V and -220V were regulated through magnetic coupling between the filtering inductors. Therefore, even for large unbalanced load condition, the output voltages stay balanced. The control voltage loop used regulates the total voltage, that is, the sum of the two DC outputs.

The command circuit was implemented with only one integrated circuit PS-PWM. Therefore, the prototype became very simple and robust. The switches are driven by pulse-transformers with positive and negative voltage pulses, minimizing the possibility of short-circuit on the switches in the same leg.

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